

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	97470	(multiplexer)	USPAT	OR	ON	2008/09/22 10:39
L2	7967	(multiplexer\$1) AND (((multiple) or (plural \$5) or (several)) adj ((input\$1) or (channel \$1))) AND ((memor \$4) or (FIFO\$1) or (buffer\$1) or (queue \$1) or (register\$1)) AND (((multiple) or (plural\$5) or (several)) adj ((output \$1) or (channel\$1)))	USPAT	OR	ON	2008/09/22 10:39
L3	1143	(multiplexer\$1) AND (((multiple) or (plural \$5) or (several)) adj ((input\$1) or (channel \$1))) AND ((memor \$4) or (FIFO\$1) or (buffer\$1) or (queue \$1) or (register\$1)) AND (((multiple) or (plural\$5) or (several)) adj ((output \$1) or (channel\$1))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit)) or (MSB))	USPAT	OR	ON	2008/09/22 10:39

L4	572	(multiplexer\$1) AND (((multiple) or (plural \$5) or (several)) adj ((input\$1) or (channel \$1))) AND ((memor \$4) or (FIFO\$1) or (buffer\$1) or (queue \$1) or (register\$1)) AND (((multiple) or (plural\$5) or (several)) adj ((output \$1) or (channel\$1))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit)) or (MSB)) AND (priorit\$3)	USPAT	OR	ON	2008/09/22 10:39
L5	248	(multiplexer\$1) AND (((multiple) or (plural \$5) or (several)) adj ((input\$1) or (channel \$1))) AND ((memor \$4) or (FIFO\$1) or (buffer\$1) or (queue \$1) or (register\$1)) AND (((multiple) or (plural\$5) or (several)) adj ((output \$1) or (channel\$1))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit)) or (MSB)) AND (priorit\$3) AND (((direct) adj (memory) adj (access)) or (DMA))	USPAT	OR	ON	2008/09/22 10:39

L6	89	(multiplexer\$1) AND (((multiple) or (plural \$5) or (several)) adj ((input\$1) or (channel \$1))) AND ((memor \$4) or (FIFO\$1) or (buffer\$1) or (queue \$1) or (register\$1)) AND (((multiple) or (plural\$5) or (several)) adj ((output \$1) or (channel\$1))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit)) or (MSB)) AND (priorit\$3) AND ((((direct) adj (memory) adj (access)) or (DMA)) near1 ((controller\$1) or (manager\$1) or (unit\$1)))	USPAT	OR	ON	2008/09/22 10:39
L7	14	(multiplexer\$1) AND (((multiple) or (plural \$5) or (several)) adj ((input\$1) or (channel \$1))) AND ((memor \$4) or (FIFO\$1) or (buffer\$1) or (queue \$1) or (register\$1)) AND (((multiple) or (plural\$5) or (several)) adj ((output \$1) or (channel\$1))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit)) or (MSB)) AND (priorit\$3) AND ((((direct) adj (memory) adj (access)) or (DMA)) near1 ((controller\$1) or (manager\$1) or (unit\$1))) AND (((input) or (source) or (channel)) adj	USPAT	OR	ON	2008/09/22 10:39

		((identifier) or (identification) or (ID)))				
L8	25	(multiplexer\$1) AND (((multiple) or (plural \$5) or (several)) adj ((input\$1) or (channel \$1))) AND ((memor \$4) or (FIFO\$1) or (buffer\$1) or (queue \$1) or (register\$1)) AND (((multiple) or (plural\$5) or (several)) adj ((output \$1) or (channel\$1))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit)) or (MSB)) AND (priorit\$3) AND ((((direct) adj (memory) adj (access)) or (DMA)) near1 ((controller\$1) or (manager\$1) or (unit\$1))) AND (((input) or (source) or (channel)) adj2 ((identifier) or (identification) or (ID)))	USPAT	OR	ON	2008/09/22 10:39
L9	13	(multiplexer\$1) AND (((multiple) or (plural \$5) or (several)) adj ((input\$1) or (channel \$1))) AND ((memor \$4) or (FIFO\$1) or (buffer\$1) or (queue \$1) or (register\$1)) AND (((multiple) or (plural\$5) or (several)) adj ((output \$1) or (channel\$1))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit)) or (MSB)) AND	USPAT	OR	ON	2008/09/22 10:39

		(priorit\$3) AND ((((direct) adj (memory) adj (access)) or (DMA)) near1 ((controller\$1) or (manager\$1) or (unit\$1))) AND (((input) or (source) or (channel)) adj2 ((identifier) or (identification) or (ID))) AND ((output) adj ((memor\$4) or (FIFO \$1) or (buffer\$1) or (queue\$1) or (register \$1)))				
L10	16	(multiplexer\$1) AND (((multiple) or (plural \$5) or (several)) adj ((input\$1) or (channel \$1))) AND ((memor \$4) or (FIFO\$1) or (buffer\$1) or (queue \$1) or (register\$1)) AND (((multiple) or (plural\$5) or (several)) adj ((output \$1) or (channel\$1))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit)) or (MSB)) AND (priorit\$3) AND ((((direct) adj (memory) adj (access)) or (DMA)) near1 ((controller\$1) or (manager\$1) or (unit\$1))) AND (((input) or (source) or (channel)) adj2 ((identifier) or (identification) or (ID))) AND ((output) near2 ((memor\$4) or (FIFO \$1) or (buffer\$1) or (queue\$1) or (register \$1)))	USPAT	OR	ON	2008/09/22 10:39

L11	25	(multiplexer\$1) AND (((multiple) or (plural \$5) or (several)) adj ((input\$1) or (channel \$1))) AND ((memor \$4) or (FIFO\$1) or (buffer\$1) or (queue \$1) or (register\$1)) AND (((multiple) or (plural\$5) or (several)) adj ((output \$1) or (channel\$1))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit)) or (MSB)) AND (priorit\$3) AND ((((direct) adj (memory) adj (access)) or (DMA)) near1 ((controller\$1) or (manager\$1) or (unit\$1))) AND (((input) or (source) or (channel)) adj2 ((identifier) or (identification) or (ID)))	USPAT	OR	ON	2008/09/22 10:39
L12	110	(multiplexer\$1) AND (((multiple) or (multi) or (plural\$5) or (several)) adj ((input\$1) or (channel \$1))) AND ((memor \$4) or (FIFO\$1) or (buffer\$1) or (queue \$1) or (register\$1)) AND (((multiple) or (multi) or (plural\$5) or (several)) adj ((output\$1) or (channel\$1))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit)) or (MSB)) AND (priorit\$3) AND ((((direct) adj	USPAT	OR	ON	2008/09/22 10:39

		(memory) adj (access)) or (DMA) near1 ((controller\$1) or (manager\$1) or (unit\$1)) or (DMAC)				
L13	46	(multiplexer\$1) AND (((multiple) or (multi) or (plural\$5) or (several)) adj ((input\$1) or (channel \$1))) AND ((memor \$4) or (FIFO\$1) or (buffer\$1) or (queue \$1) or (register\$1)) AND (((multiple) or (multi) or (plural\$5) or (several)) adj ((output\$1) or (channel\$1))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit)) or (MSB)) AND (priorit\$3) AND ((((direct) adj (memory) adj (access)) or (DMA) near1 ((controller\$1) or (manager\$1) or (unit\$1)) or (DMAC) AND (((input) or (source) or (channel)) near2 ((identifier) or (identification) or (ID)))	USPAT	OR	ON	2008/09/22 10:39
L14	45	(multiplexer\$1) AND (((multiple) or (multi) or (plural\$5) or (several)) adj ((input\$1) or (channel \$1))) AND ((memor \$4) or (FIFO\$1) or (buffer\$1) or (queue \$1) or (register\$1)) AND (((multiple) or (multi) or (plural\$5) or (several)) adj ((output\$1) or	USPAT	OR	ON	2008/09/22 10:39

		(channel\$1))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit)) or (MSB)) AND (priorit\$3) AND ((((direct) adj (memory) adj (access)) or (DMA)) near1 ((controller\$1) or (manager\$1) or (unit\$1)) or (DMAC)) AND (((input) or (source) or (channel)) near2 ((identifier) or (identification) or (ID)))AND (((output) or (transmit\$4)) near2 ((memor\$4) or (FIFO \$1) or (buffer\$1) or (queue\$1) or (register \$1)))				
L15	45	(multiplexer\$1) AND (((multiple) or (multi) or (plural\$5) or (several)) adj ((input\$1) or (channel \$1))) AND ((memor \$4) or (FIFO\$1) or (buffer\$1) or (queue \$1) or (register\$1)) AND (((multiple) or (multi) or (plural\$5) or (several)) adj ((output\$1) or (channel\$1))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit)) or (MSB)) AND (priorit\$3) AND ((((direct) adj (memory) adj (access)) or (DMA)) near1 ((controller\$1) or (manager\$1) or	USPAT	OR	ON	2008/09/22 10:39

		(unit\$1)) or (DMAC)) AND (((input) or (source) or (channel)) near2 ((identifier) or (identification) or (ID)))AND (((output) or (transmit\$4) or (transmission)) near2 ((memor\$4) or (FIFO \$1) or (buffer\$1) or (queue\$1) or (register \$1)))				
L16	45	(multiplexer\$1) AND (((multiple) or (multi) or (plural\$5) or (several)) adj ((input\$1) or (channel \$1))) AND ((memor \$4) or (FIFO\$1) or (buffer\$1) or (queue \$1) or (register\$1)) AND (((multiple) or (multi) or (plural\$5) or (several)) adj ((output\$1) or (channel\$1))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit)) or (MSB)) AND (priorit\$3) AND ((((direct) adj (memory) adj (access)) or (DMA)) near1 ((controller\$1) or (manager\$1) or (unit\$1)) or (DMAC)) AND (((input) or (source) or (channel)) near2 ((identifier) or (identification) or (ID)))AND (((output) or (transmit\$4) or (transmission)) near2 ((memor\$4) or (FIFO \$1) or (buffer\$1) or	USPAT	OR	ON	2008/09/22 10:39

		(queue\$1) or (register \$1)))				
L17	2030	((370/535) or (370/536) or (370/537) or (370/539) or (370/540) or (370/541) or (370/542) or (370/544)).CCLS.	USPAT; USOCR	OR	OFF	2008/09/22 10:39
L18	952	(370/535).CCLS.	USPAT; USOCR	OR	OFF	2008/09/22 10:39
L19	273	(370/536).CCLS.	USPAT; USOCR	OR	OFF	2008/09/22 10:39
L20	650	(370/537).CCLS.	USPAT; USOCR	OR	OFF	2008/09/22 10:39
L21	138	(370/539).CCLS.	USPAT; USOCR	OR	OFF	2008/09/22 10:39
L22	116	(370/540).CCLS.	USPAT; USOCR	OR	OFF	2008/09/22 10:39
L23	71	(370/541).CCLS.	USPAT; USOCR	OR	OFF	2008/09/22 10:39
L24	152	(370/542).CCLS.	USPAT; USOCR	OR	OFF	2008/09/22 10:39
L25	41	(370/544).CCLS.	USPAT; USOCR	OR	OFF	2008/09/22 10:39

9/ 22/ 2008 12:05:04 PM

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